AN INVESTIGATION OF COMMON EMITTER CURRENT GAIN IN LATERAL TRANSISTORS

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by
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Kanpur

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CERTIFICATE

Certified that the work entitled ''AN INVESTIGATION OF COMMON EMITTER CURRENT GAIN IN LATERAL TRANSISTORS'' has been carried out under my supervision and it has not been submitted elsewhere for a degree.

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A C K N O W L E D G M E N T S

To

- Dr M S Tyagi, my GUIDE

- ACES Engineers, particularly, Mr R S Korde

- Mr T S Kohli, Senior Research Assistant

- Mr M S Hegde, Research Scholar, Department of Chemistry

- Mr C N Krishnan, Research Scholar, Department of Electrical Engineering

- Staff of Computer Centre

- Dr M M Hasan, Integrated Circuits Laboratory

- Mr Gurcharan Singh , Foreman, Integrated Circuits Lab.

- Mr L S Gupta, Technical Assistant, and Durga Prasad, Mechanic, Integrated Circuits Lab.

and

- Mr R Pandey, Typist, Television Centre

ABSTRACT

A two dimensional analysis has been made for two lateral transistor structures. The dependencies of β with parameters like base width, junction depth, and surface recombination velocity have been evaluated for each transistor and the results are discussed. A description of fabrication technology has been presented Measurements have been made on the fabricated lateral p-n-p transistors and the results have been interpreted Verification of theoretical results with the experimental results has been attempted. Suggestions for the extension of the work have been made at the end.

CONTENTS

Chapter 1

INTRODUCTION TO LATERAL TRANSISTOR

1.1 Introductory Remarks

Lateral Transistor (LT) is a device in which the minority carrier flow in the base region is lateral unlike the case in conventional transistor in which the carrier flow is vertical. Fig. 1 shows a cross-section of two kinds of transistors, the lateral and conventional one, fabricated side by side. An obvious advantage of a lateral structure is that it immediately provides a p-n-p transistor when desired to be fabricated among n-p-n transistors with no additional processing steps. Such a need frequently arises in ICs. The disadvantages of LT structure are its low common emitter current gain (β), and low f_T. The low β results from the large base width which is limited by the photolithography to about 3-4 microns, and low f_T is due to large values of base resistivity and base transit time. The problems introduced by low β, however, can be overcome by improved circuit techniques [1]. The value of f_T can be increased by introducing a drift field in the base region so as to accelerate the carriers in the base region [2].

In lateral structures the carrier flow is two dimensional. In view of this, the results derived from one dimensional analysis will be in gross error, and only two

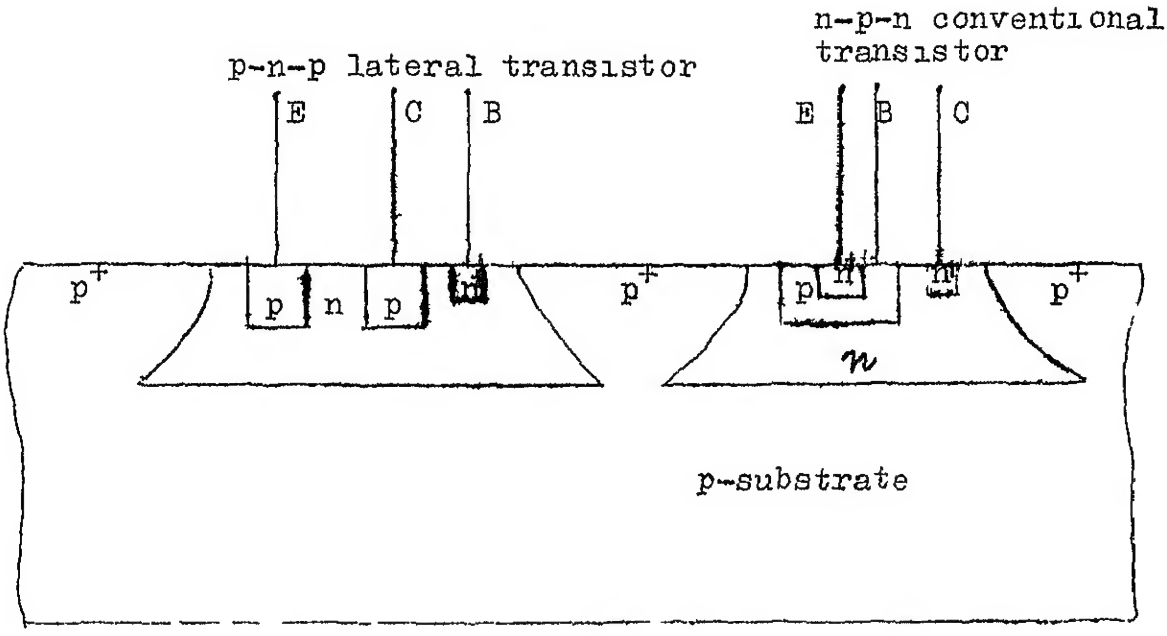


Fig. 1 A p-n-p lateral transistor fabricated simultaneously with n-p-n conventional transistor

dimensional analysis is expected to give correct results. This point has been further elaborated in Chapter 2.

1.2 Review of Development Work on Lateral Transistor

An LT structure was first proposed by Lin et al [3]. They fabricated a lateral p-n-p and a conventional n-p-n simultaneously. The value of β was about 1, and f_T was about 5 MHz. Lindmayer et al [4] however showed that by introducing an n^+ layer immediately below the emitter, β can be improved atleast by a factor of 2. Nevertheless, the value of f_T was not improved until it was shown [5] that a horizontal drift field in the base can increase f_T by a factor of 10 (i.e., from 5MHz to 50 MHz). The presence of horizontal field increases not only f_T, but also the injection efficiency by debiasing the bottom of the emitter, and increasing the bias at the vertical walls of the emitter [1]. Furthermore, it has also been shown that the introduction of an n^+ layer below the emitter need not necessarily improve β as was shown in Ref.[4].

An LT structure is primarily used in linear ICs. The unusual switching phenomena observed in IC leteral transistors, however, has been suggested for possible applications such as relaxation oscillators, over load protection circuit etc.[7].

Although LT structure has been widely used, there has so far been no detailed analysis that predicts how β

is influenced by transistor geometry and surface conditions.

1.3 Objectives of the Present Work

The present work was started with two objectives: i) to develop a technology for fabricating LT in the laboratory, and ii) to carryout a two dimensional analysis of lateral transistor and verify the results of the analysis by making measurements on the units fabricated in the laboratory.

Chapter 2 describes the one dimensional and two dimensional analyses of LT. The fabrication technology of LT is presented in Chapter 3. In Chapter 4 the results of measurements on the fabricated units are discussed. The verification of theoretical value of β with measured one is attempted in Chapter 5. Suggestions for future work are made at the end.

Chapter 2

THEORY OF LATERAL TRANSISTORS

2.1 Basic Equation for Carrier flow in the Base Region

The basic equation for the carrier profile in the base region is the continuity equation The solution of the continuity equation is strongly dependent on the geometry of the base and the boundary conditions. For the present study, the geometry shown in Fig. 2 is assumed, and the generalized continuity equation can be easily derived, from the basic equations, in the normalized form,

$$a_1 \frac{\partial^2 p_n}{\partial X^2} - a_2 \frac{\partial p_n}{\partial X} + a_3 \frac{\partial^2 p_n}{\partial Y^2} - a_4 \frac{\partial p_n}{\partial Y}$$

$$- a_5 p_n = a_6 \frac{\partial p_n}{\partial T} \qquad \ldots \qquad (2.1)$$

where

$$a_1 = 1, \; a_2 = \frac{\mu_p E_X W_x}{D_p}, \; a_3 = \frac{W_x^2}{W_y^2}$$

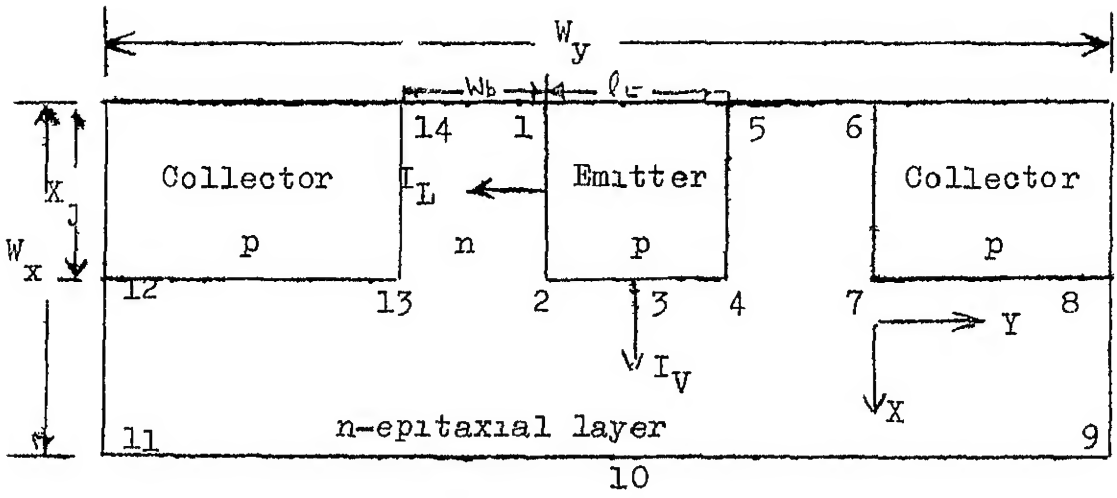
$$a_4 = \frac{\mu_p E_Y W_x^2}{D_p W_y}, \; a_5 = \frac{W_x^2}{D_p \tau_p}, \; a_6 = \frac{W_x^2}{\tau D_p}.$$

In these relations, the following notations have been used. p_n - normalized hole concentration, $= \frac{p(x,y)-p_o}{p_e(o)}$

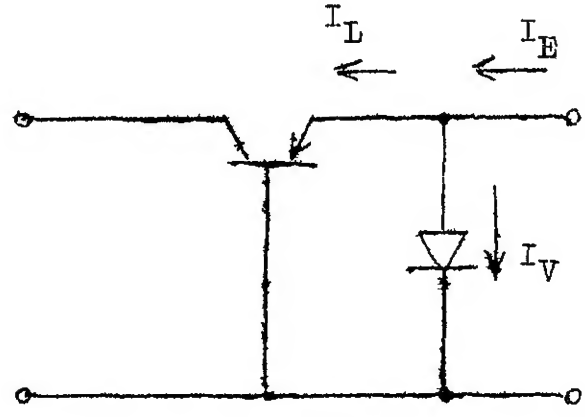
X - normalized x co-ordinate, $= \frac{x}{W_x}$

Y - normalized y co-ordinate, $= \frac{y}{W_y}$

T - normalized time (t) co-ordinate , $= \frac{t}{\tau}$



(a)



(b)

Fig. 2 Lateral transistor (LT) structure (a) Cross-section, (b) equivalent Circuit

τ - a convenient time constant

E_X - field component along X-axis

E_y - field component along Y - axis

W_x and W_y are the dimensions of the transistor (Fig. 2). Other symbols carry the usual meaning.

An analytical solution for Eq. 2.1 in the base region bounded by 1-2-3-4-5-6-7-8-9-10-11-12-13-14 would obviously be impossible. A simple solution is provided by a quasi-two dimensional analysis [8,4], assuming the following:

i) the hole component of the emitter current is separable into two parts, I_L and I_V (Fig. 2).

ii) $E_X = E_Y = 0$.

iii) there is no recombination in the base.

Under steady state conditions, Eq. 2.1 can then be written as,

$$C_1 \frac{\partial^2 p_n}{\partial Z^2} = 0 \qquad \ldots\ldots\ldots\ldots\ldots 2.2$$

where $C_1 = a_1$, and $Z = X$ for I_V, and

$C_1 = a_3$, and $Z = Y$ for I_L.

Thus, the carrier profile, as described by Eq. 2.2, is a straight line in both X and Y directions. Further, assuming that the carrier gradients along X and Y directions are given by $\frac{p_e(o)}{L_p}$ and $\frac{p_e(o)}{W_b}$ respectively, I_L and I_V can be expressed as

$$I_L = - \frac{q D_p X_J L_E p_e(o)}{W_b}, \text{ and}$$

$$I_V = - \frac{q D_p J_E L_E p_e(o)}{L_p} .$$

The equivalent emitter efficiency of the transistor[Fig. 2 (b)] would be,

$$\gamma = \frac{I_L}{I_L + I_V}$$

Since the base transport factor $\beta = \text{sech} \frac{W_b}{L_p}$, the common emitter current gain β can be approximately written as [8],

$$\frac{1}{\beta} = \frac{1}{X_J} \frac{W_b}{L_p} + \frac{W_b^2}{2L_p^2} + \frac{1}{2L_p^2} \frac{W_b^3}{X_J} \quad . \quad . \quad . \quad 2.3$$

It will be shown later in this Chapter that, in spite of the gross assumptions, Eq. 2.3 not only predicts the value of β with enough accuracy, but also the variation of β with base width. Eq. 2.3, however, does not mention how the surface conditions affect β. Moreover, the X_J dependence of β predicted by this equation, as has been shown later in this Chapter, is not in agreement with a more correct two dimensional analysis.

2.2 Two Dimensional Analysis

A more accurate analysis which overcomes the above inadequacies can be made by numerically solving Eq. 2.1 with appropriate boundary conditions. For the geometry

shown in Fig. 2(a) the boundary conditions are:

i) $p_n = 1$ along 1-2-3-4-5

ii) $\frac{\partial p_n}{\partial X} = 0$ along 14-1, and 5-6

iii) $p_n = -\frac{p_o}{p_e(o)}$ along 12-13-14, and 6-7-8

iv) $\frac{\partial p_n}{\partial Y} = 0$ along 11-12, and 8-9

v) $p_n = 0$ along 11-10-9 when the base contact is taken from the bottom of the substrate. When the contact is taken, however, from the top (as in IC fabrication) then $\frac{\partial p_n}{\partial X} = 0$ along 11-10-9.

When the surface recombination velocity is non-zero, the boundary condition (ii) becomes

$\frac{\partial p_n}{\partial X} = \frac{p_n v_{sr}}{D_p}$, where v_{sr} is the surface recombination velocity.

2.2.1 Steady State Condition

For steady state, the carrier distribution in the base region can be obtained by setting $\frac{\partial p_n}{\partial T} = 0$ in Eq. 2.2, and solving the resulting equation by employing the finite difference scheme. The equivalent difference equation of the resulting relation can be written as

$$e_1 p_{i-1,j} + e_2 p_{i,j} + e_3 p_{i+1,j} + e_4 p_{i,j-1} + e_5 p_{i,j+1} = 0 \qquad \ldots\ldots\ldots\ldots 2.4$$

where the subscript n has been dropped for convenience, and

$$e_1 = \frac{a_3}{h_y^2} + \frac{a_4}{2h_y} h_x^2 , \quad e_2 = -2a_1 - 2a_3 \frac{h_x^2}{h_y^2}$$

$$- a_5 h_x^2,$$

$$e_3 = \frac{a_3}{h_y^2} - \frac{a_4}{2h_y} h_y^2, \quad e_4 = a_1 + a_2 \frac{h_x}{2}$$

$$e_5 = a_1 - \frac{a_2 h_x}{2} ,$$

h_x and h_y being the step size in X and Y directions respectively.

The base region is divided into a number of meshes, each of size $h_x \times h_y$, and the difference equation (Eq. 2.4) is written at all the corner points of every mesh. This would result in a system of simultaneous equations with as many variables as there are points in the base region. The coefficient matrix of the set of equations is highly sparse. The diagonal dominance of the matrix is sufficiently large to enhance the rate of convergence of any iteration scheme that may be used to solve the set of equations.

A straight forward method to obtain the carrier distribution in the base region would be to solve the time dependent continuity equation using the Explicit Method [9], and let t tend to a large value so that the

steady state is reached The time step involved in this method is so small (10^{-6}) that it would take a prohibitively large number of iterations to reach the steady state. An improved and the fastest algorithm that may next be tried out is the so called Alternating Implicit Direction (AID) method [9]. Though this method is very attractive for its simplicity and fastness, the constraints imposed by it for its convergence are very rarely satisfied in practical cases. For the base region involved in this work, this method was tried out and was found absolutely useless. The next hopeful algorithm is SOR (Successive Over Relaxation)Method. The optimum relaxation factor for SOR method was obtained by actually solving the system of equations in computer for different relaxation factors, and was found to be 1.3. The results of the computations are discussed below. The calculations were carried out assuming $E_X = E_Y = 0$ for two transistors,one, with base contact taken from the top as is usual in ICs (ICT), and the other, with base contact taken from the bottom below the emitter and collector (BCT).

2.2.2 Results of Computations And Discussions

The carrier profile obtained from the two dimensional analysis are shown in Fig. 3 and Fig. 4. It can be seen that for BCT most of the emitter current flows down

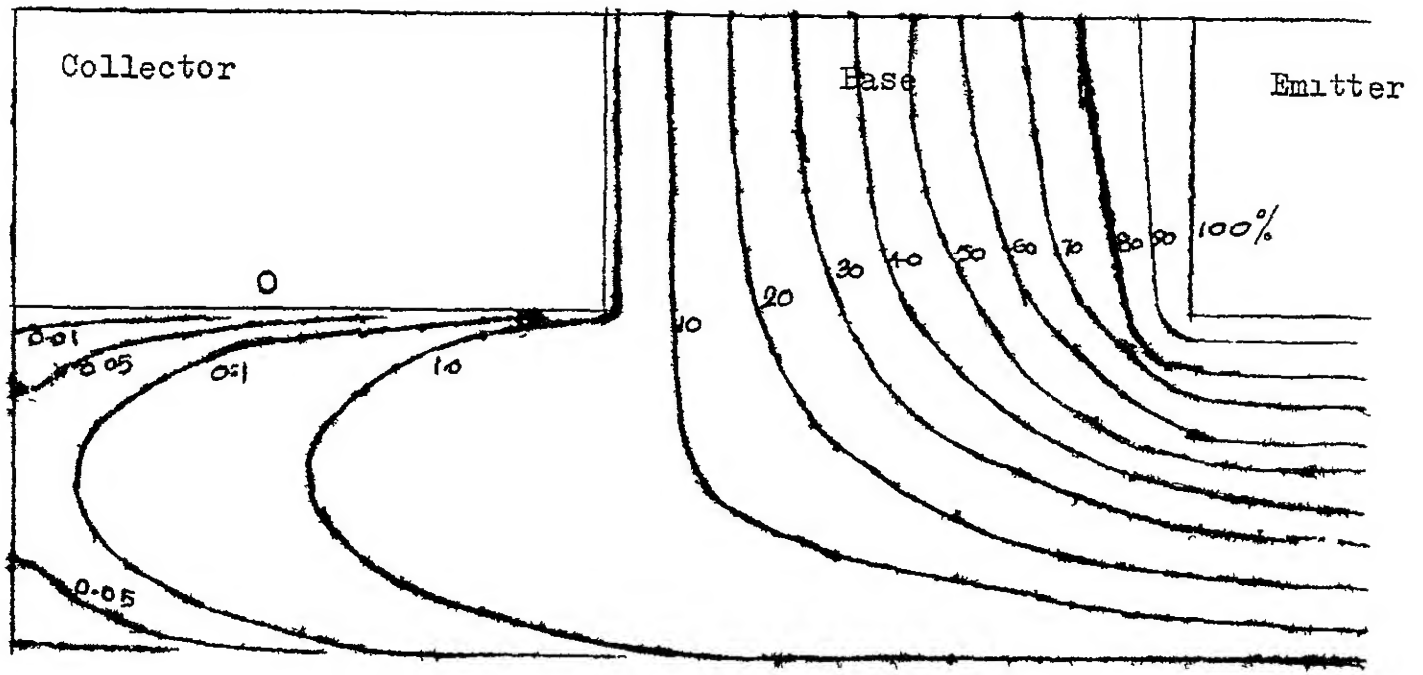


Fig. 3 Carrier distribution in the base region of BCT

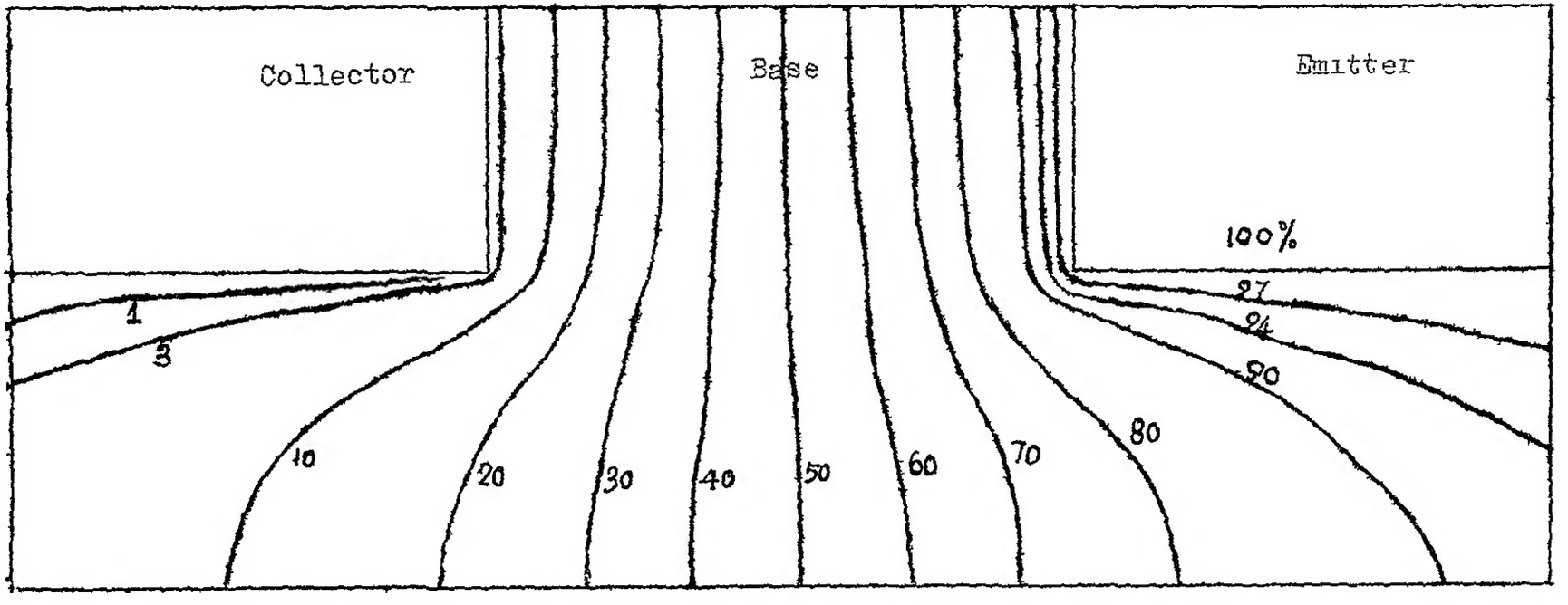


Fig. 4 Carrier distribution in the base region of ICT

to the base contact. The lateral component of the current collected at the vertical collector walls is small, and an insignificantly small number of carriers is collected at the bottom floor of the collector. When the base contact is taken at the top, the base current is drastically reduced. For a junction depth equal to 50 percent of epitaxial layer thickness, β was found to improve from 0.8 to 3.4 when the base contact was taken from the top instead of from the bottom.

A theoretical plot of β Vs log V_{sr} exhibits the bell shaped variation as shown in Fig. 5. It is seen that the variation for ICT is steeper than that for BCT. This may be explained as follows. In BCT, a large portion of the emitter current flows down to the base contact. A small fraction of the emitter current which flows towards the collector is collected by the collector. This small fraction is very sensitive to the surface conditions Since the major portion of the emitter current flows into base contact, the dependency of the lateral component with v_{sr} is not so well exhibited. This phenomena, however is not present in ICT. Hence, β Vs log v_{sr} is steeper for ICT than that for BCT. It is further to be noted that for ICT structure β becomes almost insensitive to v_{sr} for values of v_{sr} in excess of 10^3 m/sec. In practical devices, the surface is cleaned by chemical etching

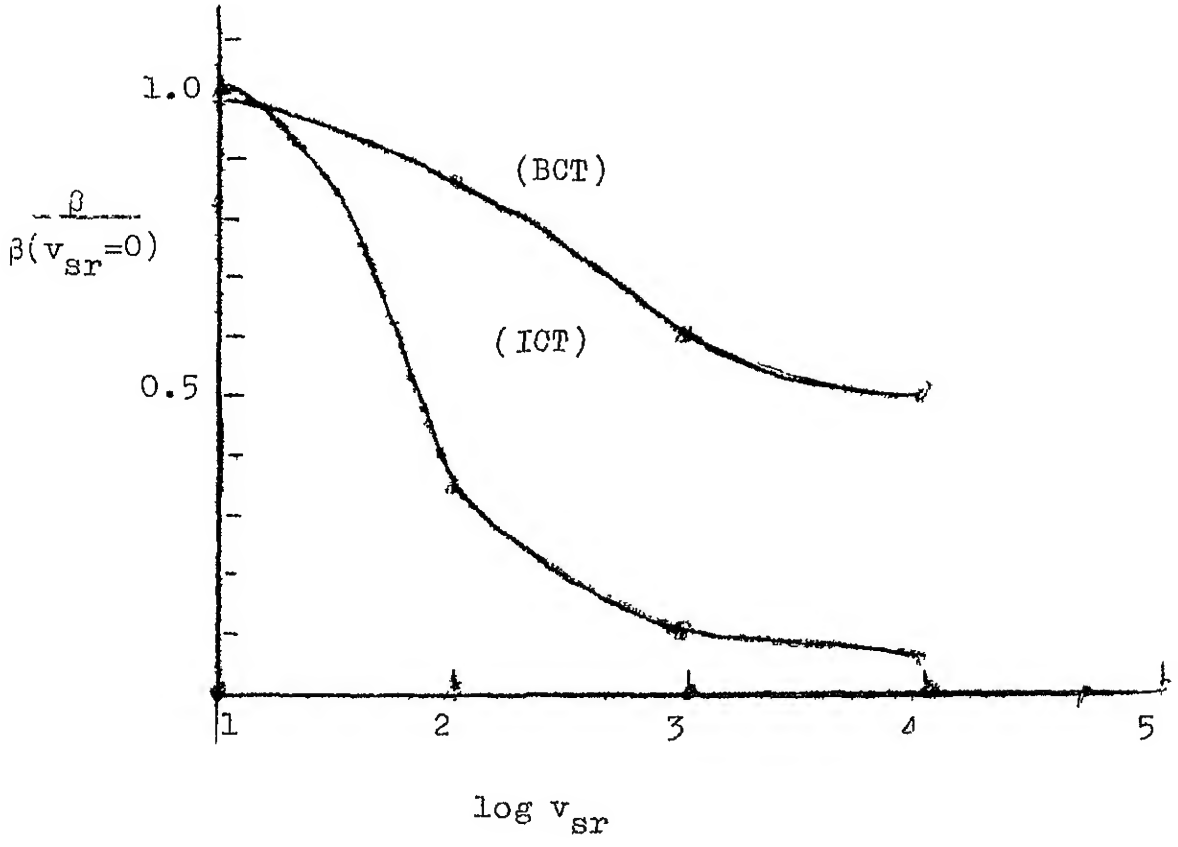


Fig. 5 Effect of v_{sr} on β for BCT and ICT structures

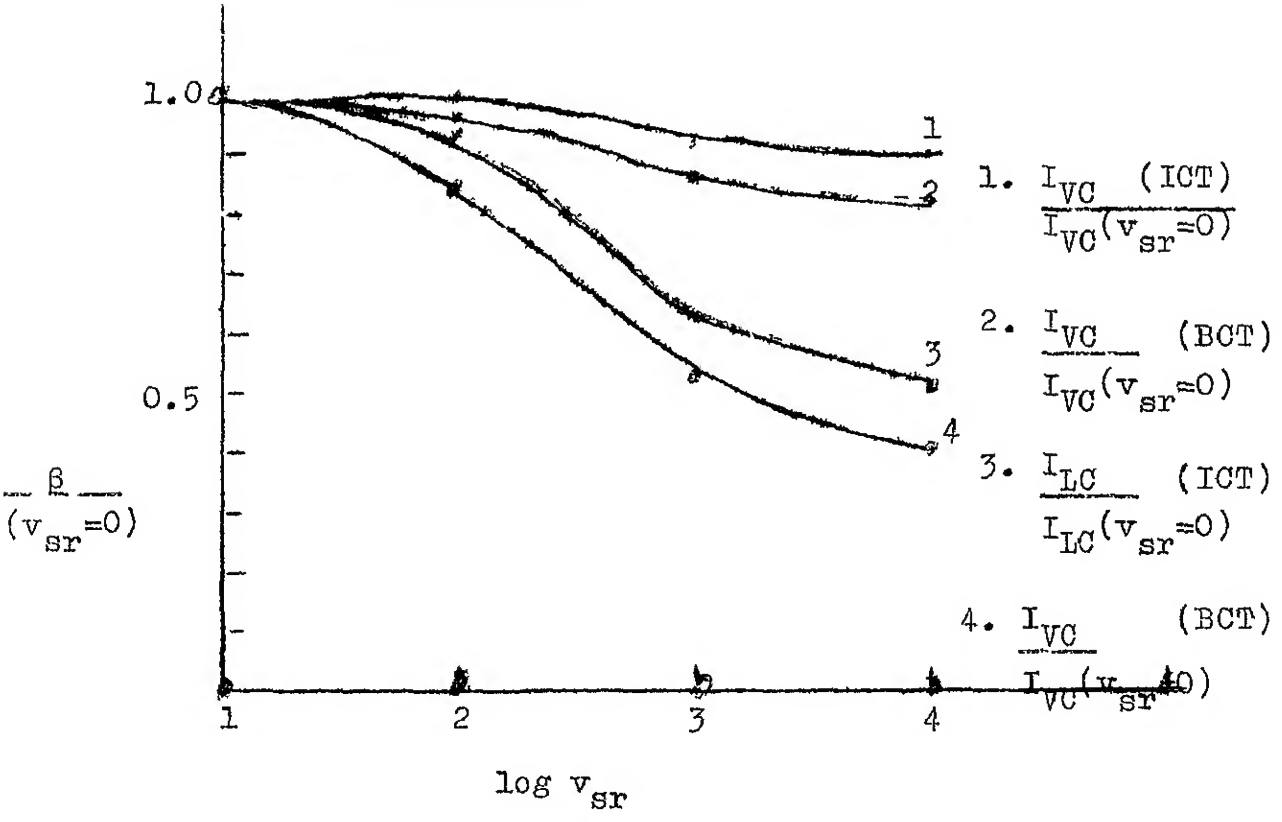


Fig. 6 Lateral component of collector current as a function of v_{sr} for BCT and ICT structures

and polishing, and v_{sr} values are significantly less than 10^3 m/sec.

Fig. 6 shows the lateral and the vertical components of the collector current as a function of v_{sr} for the two transistors It is obvious from this figure that the lateral component has a much stronger dependence on v_{sr} than the vertical component More over, the curves for the lateral component have the shape very similar to the β Vs log v_{sr} curves of Fig. 5. It may, therefore, be concluded that the bell shaped curves of Fig. 5 results from the change in lateral current with v_{sr}.

β Vs junction depth curves of Fig. 7 exhibits a maximum for BCT. This is because when the junction depth is small lateral collection is also small, and majority of the emitted carriers go to the base contact. As the junction depth is increased gradually the lateral component increases because of the increase in lateral collector area whereas the vertical component is not changed significantly. As a result of this, β of the transistor increases and reaches its maximum value when X_J is about 0.45 W_x. When X_J is further increased the emitter junction comes closer to the base contact, and a major portion of the emitter current flows into the base terminal which in turn decreases the β of the transistor.

For ICT, β remains almost constant for junction depth less than about 0.5 W_x. The fall off of β beyond this

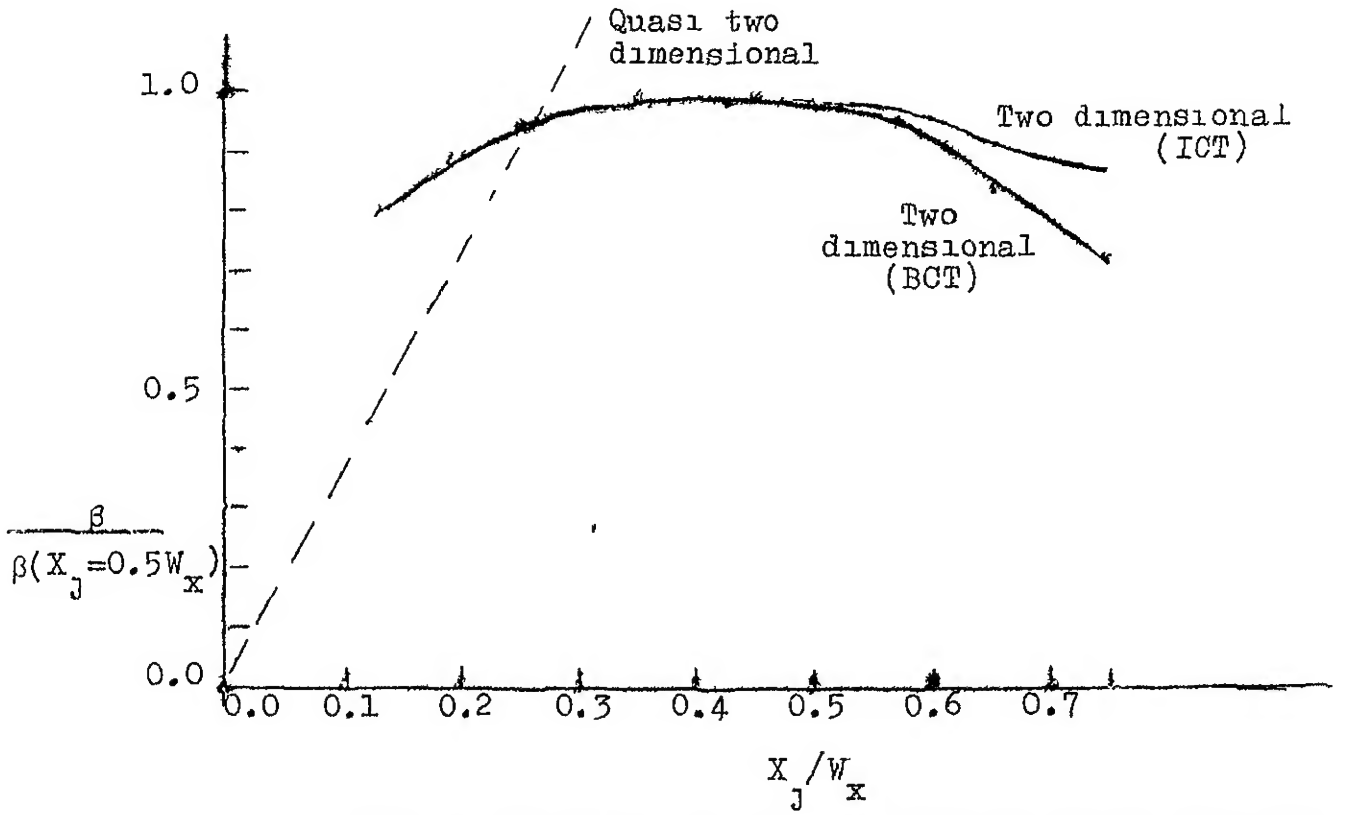


Fig. 7 Variation of β with junction depth for BCT and ICT structures

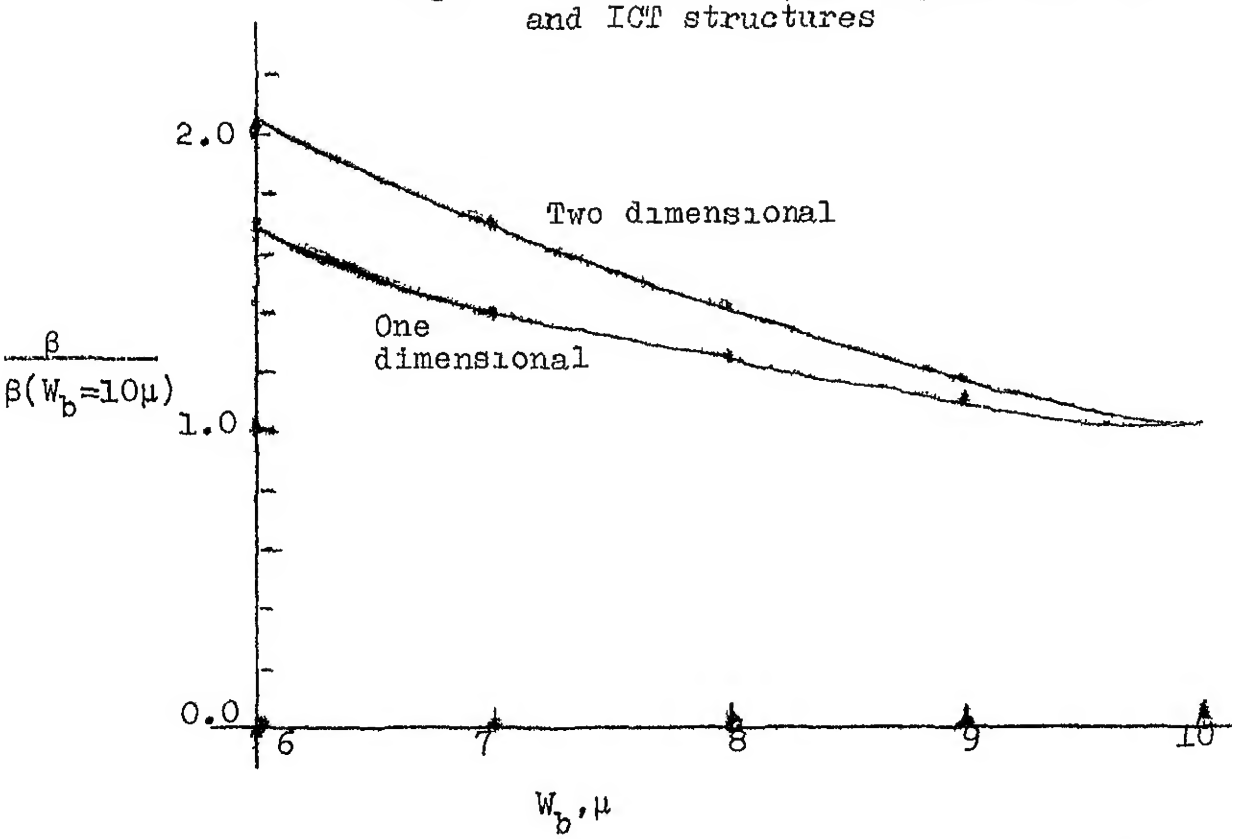


Fig. 8 β as a function of base width for BCT structure.

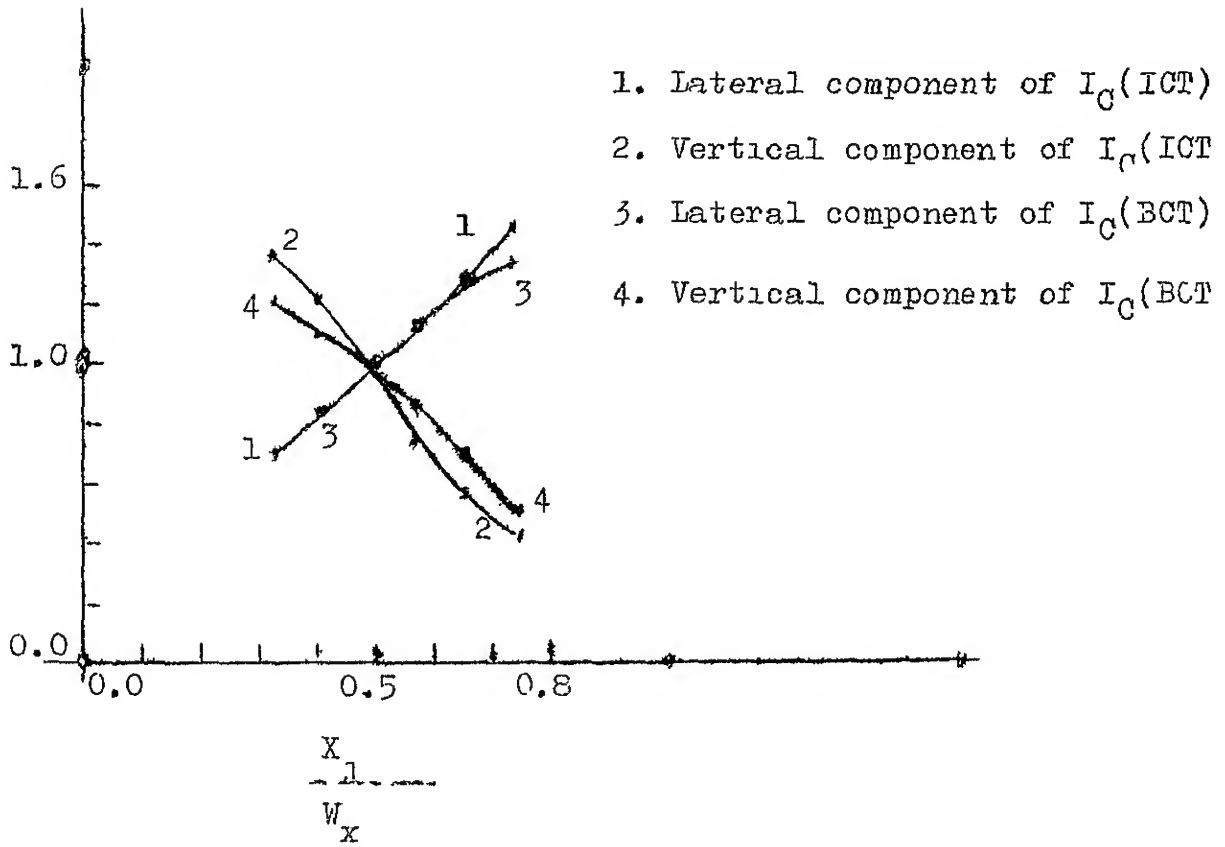


Fig. 9 Variation of the lateral and vertical components of collector current as a function of junction depth for BCT and ICT structures

point is not as sharp as that for BCT. The reason for the fall off is not known The dotted line shows the variation of β with X_J as predicted by Eq. 2.3.

β Vs base width plot of Fig. 8 is of hyperbolic nature approximately. Although this shape is approximately predicted by the quasi-two dimensional analysis [8], the predicted values of β for base widths smaller than 10 microns are significantly smaller than those obtained from the two dimensional analysis.

The lateral component of collector current varies exactly in the same manner for both BCT and ICT (Fig.9). It is interesting to note that for both the transistors the vertical and lateral components become equal at about $X_J = 0.5\ W_x$.

Chapter 3

FABRICATION TECHNOLOGY

3.1 Design Considerations

As has already been mentioned, the β of an LT can be approximately given by [8].

$$\beta = \frac{X_1}{W_b} \frac{L_p}{l_E},$$

where all the symbols have their usual meanings as explained in Chapter 2. For circular geometry l_E is replaced by r_E, the radius of the emitter. Since β varies inversely with W_b and l_E, it is advisable to keep them as small as possible. The lower limit on these is put by the process technology, particularly by the photolithography. When the work was started the author did not have much experience in photolithography and he was not sure if the resolution of the order of 5 microns could be easily achieved. It was therefore decided to keep W_b as 10 microns. The emitter contact width was also fixed at 10 microns. Consequently, the emitter width was kept at 30 microns. Since the length of the emitter does not affect β, it was chosen to be 40 microns to ease photolithography. Since W_b=10 microns the width and length of the inner collector boundaries become 50 and 60 microns respectively. Keeping a clearance of more than 10 microns around all the sides of the collector contact, and arbitrarily fixing the collector contact

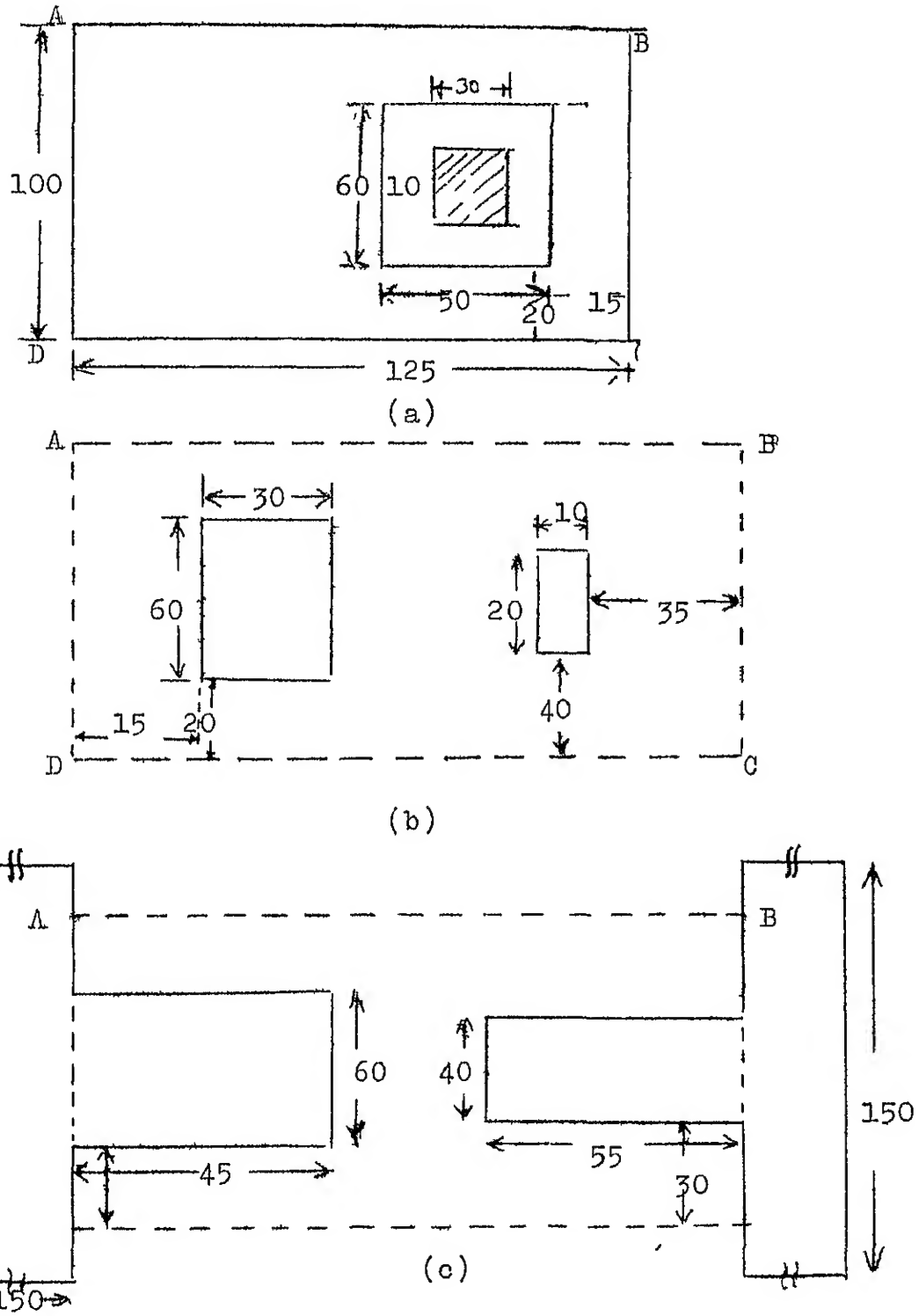


Fig. 10 Plan view of photo-masks for rectangular geometry (a) Mask pattern for emitter and collector diffusion windows , (b) Mask pattern for contact windows , (c) Mask pattern for metalization.

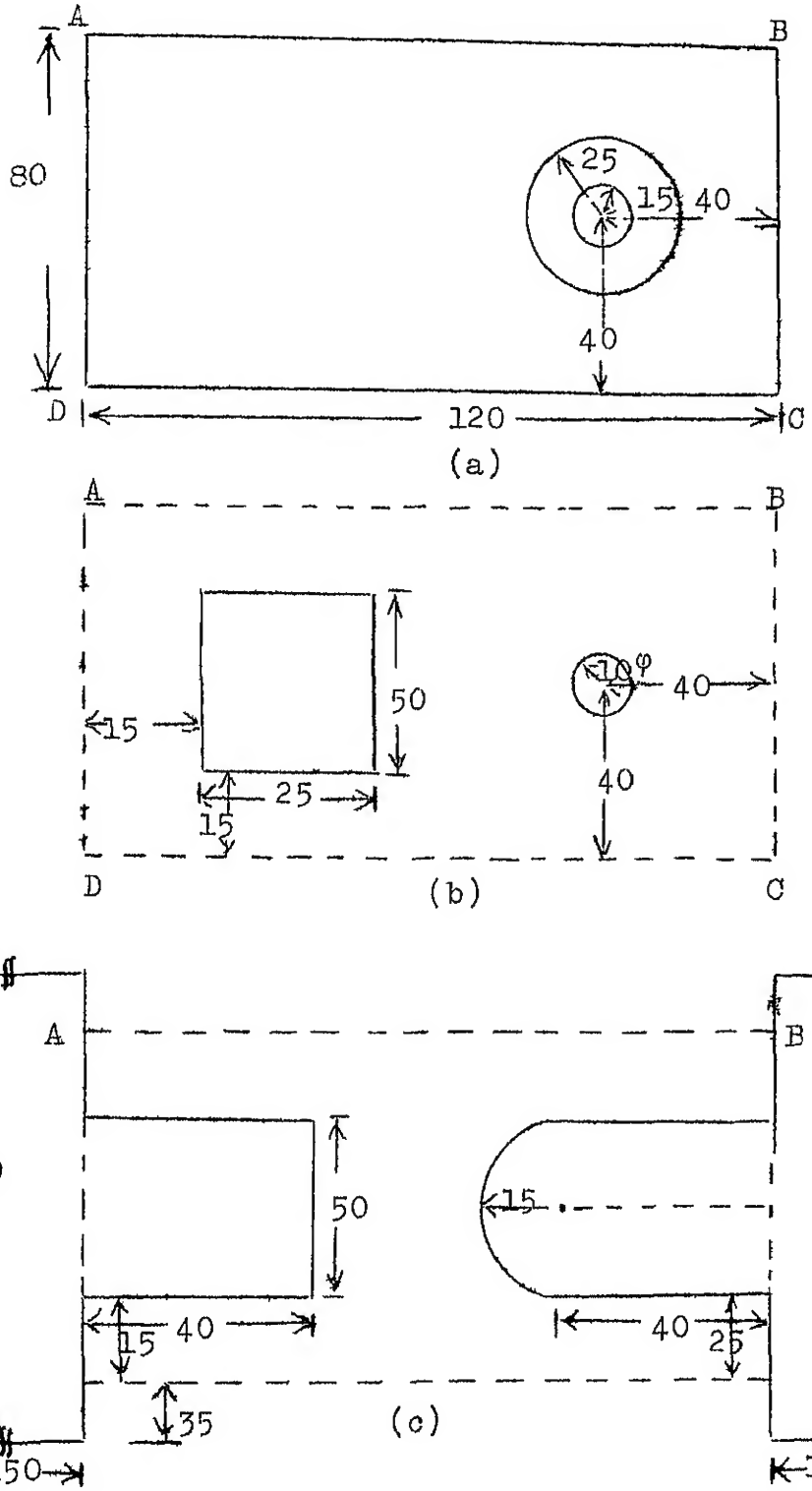


Fig. 11 Plan view of photo-mask for circular geometry
(a) Mask pattern for emitter and collector diffusion windows, (b) Mask pattern for contact windows, (c) Mask for metalization

width as 30 microns, the size of the outer collector boundary becomes 125 x 100 microns.

3.2 Making of Photo-Masks

Photo-masks for two transistor geometries (one, rectangular and other, circular) were designed and got fabricated. A third geometry which was a field aided structure was also plannel but was not fabricated because of its complexity.

Fig. 10 shows the plan view of three masks for fabrication of the lateral transistor with rectangular geometry. Fig. 11 shows similar patterns for transistor with circular geometry.

Alignment marks have also to be drawn on all the three masks for a given geometry. The marks can be of any convenient geometry and size In this work, equilateral triangles of 1 mil side were used at the four corners of the the pattern as shown in Fig. 12. With this arrangement it was found that the alignment was difficult and time consuming It is, therefore, suggested that in future works the alignment marks be kept at the corners of each device. Alternatively, the marks can also be kept around the pattern, but the distance between the adjacent marks should not be less than 1''.

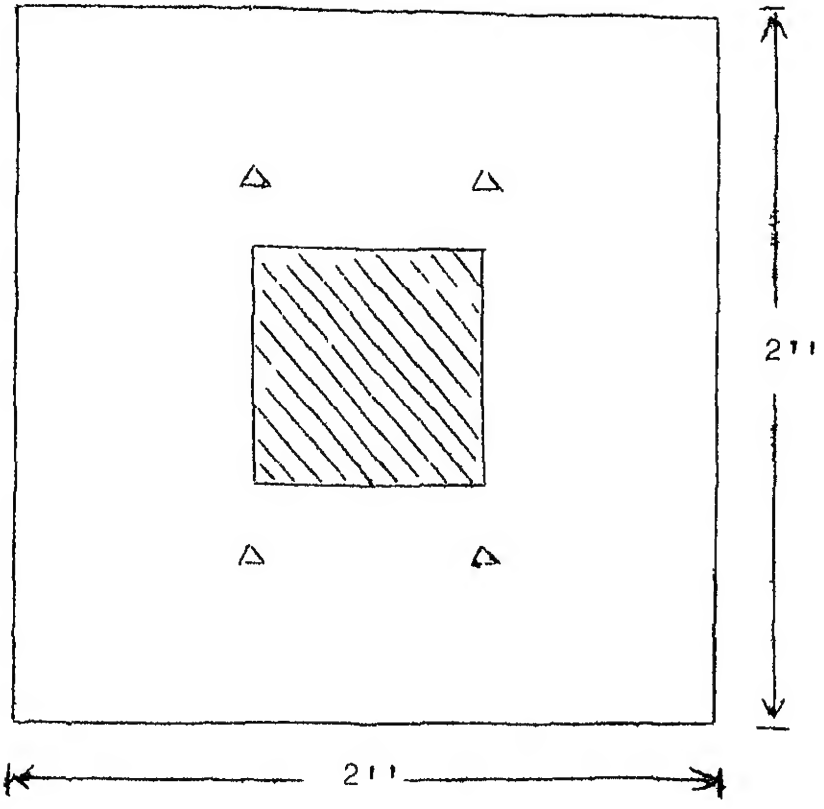


Fig. 12 Overall plan view of a slide in with alignment marks(triangles)

3.3 Device Fabrication

n-type epitaxial wafers polished on one side were used to fabricate the transistors. The resistivity of the epitaxial layer had been specified as 0.85 ohm-cm, and its thickness was around 7 microns.

3.3.1 Oxidation

As has already been mentioned in Chapter 2, the lateral component of the collector current I_C forms the major part of I_C. This component is sensitive to surface conditions. Hence, it is important to follow a good cleaning procedure before the first oxidation step.

The wafer was cleaned (The cleaning procedure given in Ref. 10 may also be used.) by boiling in sulnit solution (Conc.HNO_3 + Conc. H_2SO_4 1 1 by volume) for 5-10 mts, and rinsing in DDIW for 3-5 mts. After this, the wafer was dried using a hot blower, and transferred directly to the oxidation tube. Oxidation was carried out at 1100°C, the cycle being dry/wet/dry 60/100/60 mts. The oxygen flowrate was kept at 550 cc/mnt, and bath temperature for wet oxidation was 95°C. The thickness of the grown SiO_2 layer is not critical in this work except that it be large enough to provide effective masking against the boron diffusion in unwanted areas. Using the color chart, the thickness was estimated to be about 0.7 micron.

3 3.2 Photolithography

The first photolighography was carried out to etch out windows for emitter and collector diffusion The wafer was cleaned as before, and was thoroughly dried in an oven. It was coated with photo-resist, and exposed for 10 secs. through the emitter-collector diffusion mask Buffered etch [NH_4F plus HF (48.8 percent) in 7 1 by volume] was used for etching out windows.

3.3.3 Diffusion

After window etching, the photo-resist was stripped off, and the wafer was cleaned as before. It was dried in hot air, and was then loaded for diffusion.

a. Boron Diffusion

Boron nitride (BN) wafers were used as solid state source for p-type impurity diffusion. The BN wafers were cleaned by agitating in trichloroethylene, and then in acetone. The wafer was rinsed in DDIW, and dehydrated at about 300-400°C.

Pre-deposition was done at 900°C, for 30 mts, flowing N_2 at 550 cc/mnt. This was followed by a drive in at 1125°C for 200 mts. During drive in N_2 flow at 200 cc/mnt was maintained. In addition to this, an O_2 flow of 200 cc/mnt was also maintained to grow SiO_2 for the next photolithography.

b Measurements on Diffused Wafer

The sheet resistivity of the diffused wafer was measured by Four-Point-Probe Method, and was found to be 327.2 ohms per square. Junction depth was determined using the angle lapping method [11], and was found to be 3.2 microns. The surface concentration, for the above values of sheet resistance and junction depth, was estimated to be $4 \times 10^{17}/cm^3$ [12].

3.3.4 Contact Evaporation

After boron diffusion and second oxide layer growth, the wafer was cleaned and the contact windows were etched out using the second mask which was aligned with the help of the mask aligner. After opening the contact windows, the wafer was cleaned, and Al was evaporated for making contacts on emitter and collector regions. Evaporation was done at a typical pressure of 1×10^{-5} Torr Contact regions were etched out using metalization mask. After this, the Al contacts were alloyed at 550°C for 4-6 mts. in N_2 atmosphere. It is important that the temperature doesnot exceed 550°C, because even at temperatures as low as 560°C Al diffuses through SiO_2[13].

Chapter 4

MEASUREMENTS AND DISCUSSION OF RESULTS

Lateral transistors with circular geometry were fabricated on n-n^+ epitaxial wafers. The contact for the base was taken from the bottom of the n^+ - substrate. The results of the measurements on these transistors are described and discussed below.

4.1 Measurements of I-V Characteristics of Emitter and Collector Junctions

I-V characteristics of the emitter and collector junctions of a typical transistor are shown in Fig. 13. The forward characteristic of the emitter junction shows a cut-in voltage of about 0.5V. The reverse saturation current, I_o is about 0.7 microamp at 300°K. The reverse current I_o increases slowly as the reverse bias is increased. The knee of the break down occurs at -10V, and the junction breaks down completely at -13.5V. The large value of I_o is probably due to large surface leakage. The break down at -13.5V is quite sharp.

The collector junction exhibits approximately the same characteristics as that of the emitter junction.

4.2 Common-Emitter Characteristics

The CE characteristics, for a typical transistor, are shown in Fig. 14. The value of the common-emitter off-set voltage is about 35 mV, and the collector-to-

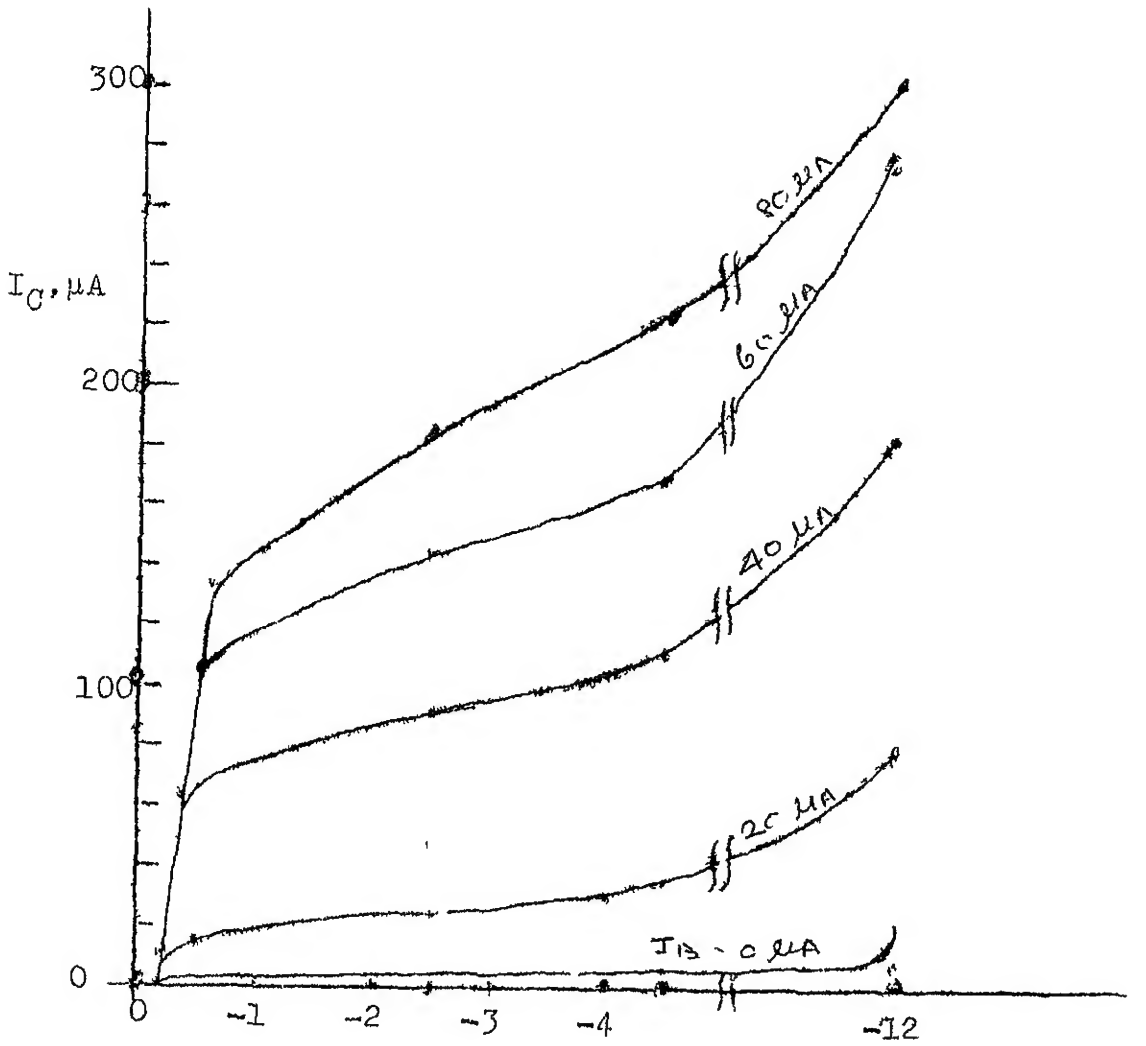


Fig. 14 Common Emitter characteristics

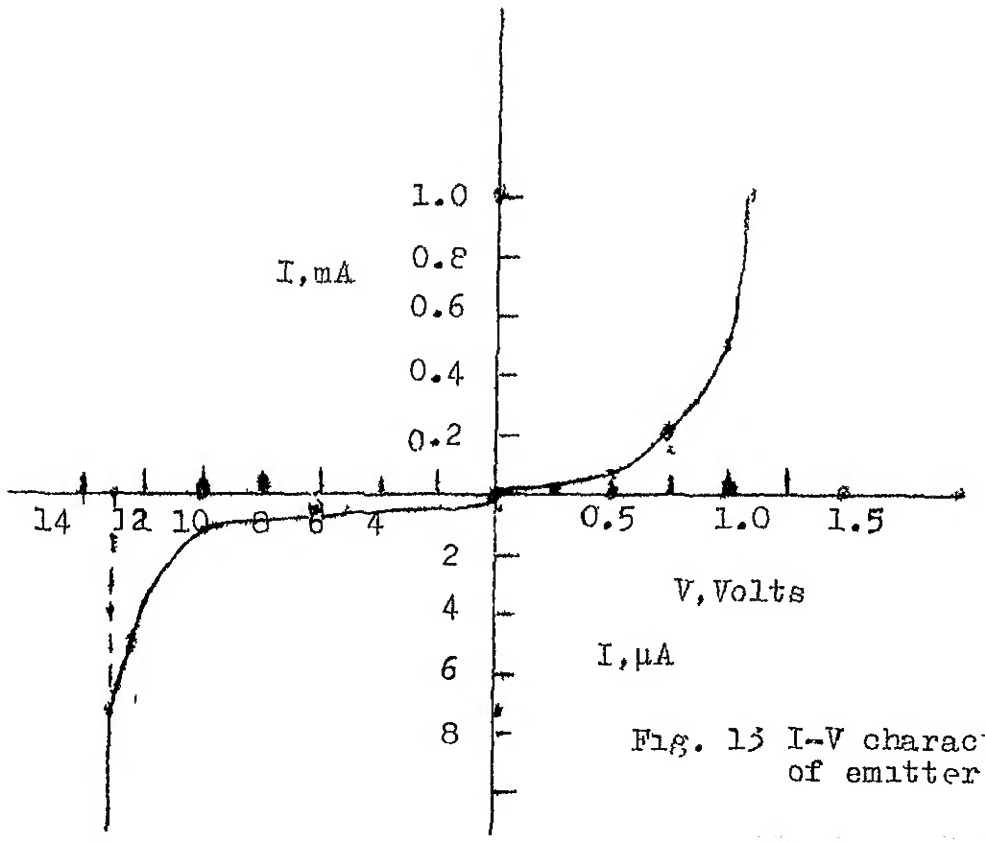


Fig. 13 I-V characteristics of emitter junction

emitter saturation voltage is 0.6V. The large value of the off-set is not surprising. For the lateral transistor the value of normal β is small, and therefore the value of inverse β is also small. The value of the saturation voltage is unusually large. This may probably be due to large collector series resistance which may partly be due to poor ohmic contacts. This point, however, was not pursued further.

4.3 Dependence of Common Emitter Current Gain on Collector Current and Collector-Emitter Voltage

a. Variation of β with I_C

The measured value of β for the fabricated transistors is typically about 1-2. Normally, for LPTs the value of β is about 5 [2]. The lower values of β obtained in our experiments are due to i) large base width (10 microns), and ii) low emitter doping ($C_o = 4 \times 10^{17}/cm^2$, $X_j = 3.2$ microns). The value of β increases with collector current I_C for low values of I_C, and falls off at large values of I_C after reaching a maximum (Fig. 15). The value of the maximum depends on the magnitude of V_{CE}. It is also evident from Fig. 15 that the maxima of β occur in the range 100-150 microamp for all values of V_{CE}. The fall off of β beyond each maximum, for a given V_{CE}, marks the on set of high injection. Hence, the fabricated lateral transistor is essentially a low current device.

The nature of variation of β with I_C (Fig. 15) is approximately the same as that of a conventional

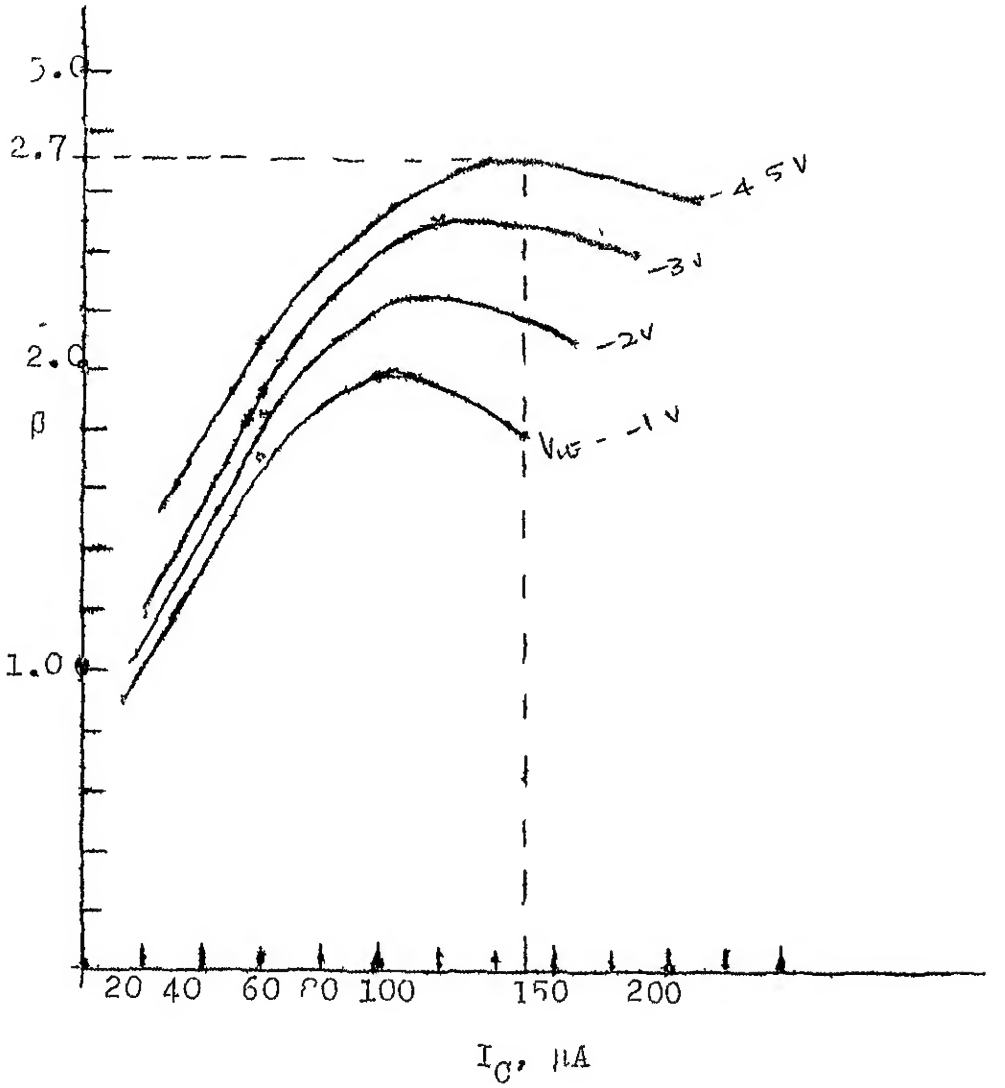


Fig. 15 Dependence of β on collector current

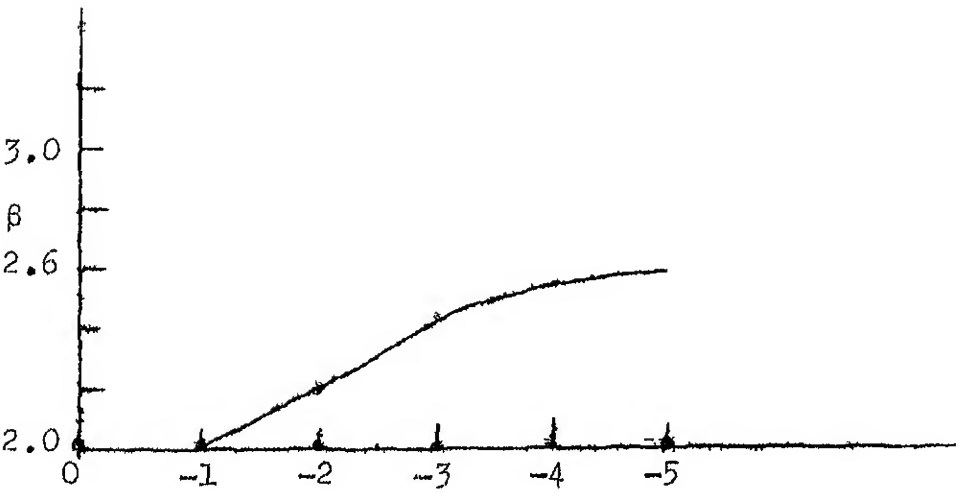


Fig. 16 Variation of β with V_{CE}

transistor. In comparison with the β of a conventional transistor, however, the β of the fabricated lateral transistor rises some what steeply with I_C for low values of I_C below the maximum point (see Fig. 15). The fact that the maximum value of β depends on V_{CE} is understandable.

b. Variation of β with V_{CE}

β may vary with V_{CE} for two reasons i) the velocity of the carriers in the collector depletion region increases with applied field.. When V_{CE} is increased the width of the collector depletion region also increases, and so does the value of electric field in the depletion region Consequently, the velocity of the carrier increases, and the carriers will be removed at a faster rate from the edge of the depletion region, ii) the active base width decreases with V_{CE} due to the extension of the depletion region into the base region. This increases the collector current for given value of emitter current, and hence the value of β increases. While the first effect is of secondary importance, the second plays a dominant role in changing the value of β.

Fig. 16 shows the variation of β with V_{CE}. The dependency is approximately linear. Strictly, it is not expected to be linear because of the nonlinear dependence of active base width (and also the velocity of the carrier in the depletion region) with V_{CE}.

Chapter 5

INTERPRETATION OF EXPERIMENTAL RESULTS AND CONCLUSIONS

5.1 Correlation of Theory and Experiment

Before attempting a comparison of theoretically calculated values of β with the measured ones, it is necessary to reiterate the assumptions which are implicitly present in the two dimensional analysis, viz.,

i) the generation-recombination and the surface leakage currents are negligible.

ii) high injection effects are absent. It was mentioned in Chapter 4 that the measured values of β depend on the collector current I_C, and that β reaches a maximum at some value of collector current. The maximum value of β is 2.7 and it occurs at I_C= 150 microamp and V_{CE} = - 4.5V. The above assumptions are reasonably valid around this value of I_C. The calculated value of β for the transistor of the same geometry (circular, epitaxial layer thickness W_x = 7 microns, and W_b = 6 microns) is 2.15. In view of all the above assumptions and uncertainty, the agreement between the measured and calculated values of β appears to be satisfactory. The value of β calculated from the quasi two dimensional analysis (Eq. 2.3) is 1.28 which is much lower than the measured value. Therefore, the two dimensional analysis gives more satisfactory result. In calculating the value of β, the effect of lateral diffusion was

taken into account [14], and when this was done the effective base width was found to be about 6 microns.

5.2 Conclusions

A two dimensional analysis was made for two types of transistor structures (ICT and BCT) with circular geometry The respective minority carrier distribution in the base region was studied and have been plotted graphically. It has been found that the value of β improves from 0,7 to 3.2 when the base contact is taken from the top rather than from the bottom of the structure.

The variation of β with log V_{sr} calculated from the two dimensional analysis showed a bell shaped curve both for BCT and ICT configurations. β of the ICT structure has been found to be more sensitive to the surface conditions.

The value of β for BCT has been shown to have much stronger dependence on junction depth than that of ICT. The variation of β with base width is hyperbolic for BCT.

Lateral p-n-p transistors were fabricated. It was found to be a low current device. The typical value of β was 1-2. The maximum value of β was 2.7, and occured at I_C = 150 microamp The nature of variation of β with I_C and V_{CE} was typical.

The measured value of β has been shown to be in good agreement with the value calculated using the two dimensional analysis. Also , the two dimensional analysis was found to be closer to the experimental results than the quasi two dimensional analysis

Many other measurements such as small signal measurements, and transient measurements were not made for lack of facilities. Further, the theoretical prediction of the variation of β with junction depth, base width and surface conditions could not have been verified for the same reason. This may become a part of future work.

5.3 Suggestions for Future Work

The following suggestions are made for the extension of the present work.

1. To verify all the theoretical curves experimentally
2. To improve the theoretical analysis to take care of high and low injection effects.
3. To propose a model for the LT and verify the validity of the model [15] for the fabricated structure.
4. To fabricate field aided lateral transistors and investigate the effect of base field on β (The effect of time varying field may be studied theoretically to see if any new kind of action is possible).

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